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# EECE 276

## Embedded Systems

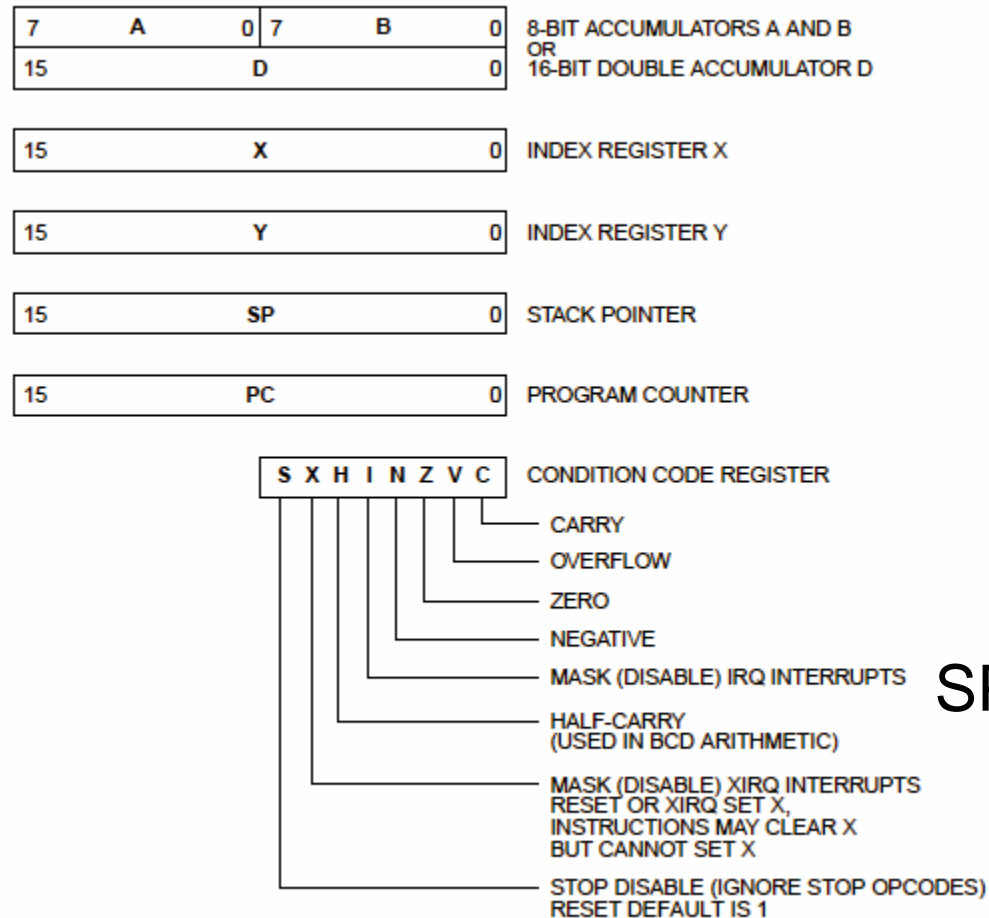
HC 12 Overview: Addressing modes,  
instructions

# HC12 Introduction

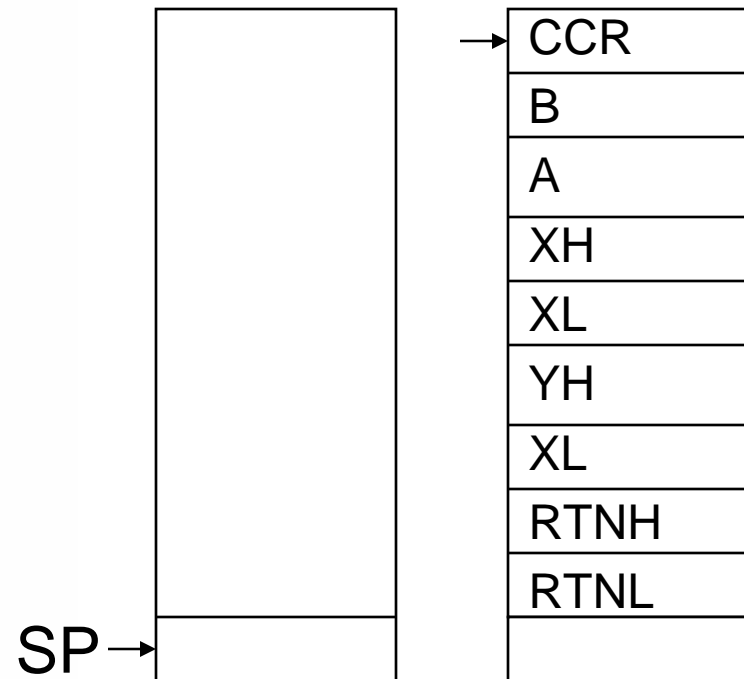
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- “Big brother” of HC11
- Source code compatibility
  - » Binary code is NOT compatible!
- Similar programmer’s model
  - » (A/B-D,X,Y,SP,PC)
- 16-bit architecture – 16 bit datapaths
- Instruction queue
  - » Pipelined cache to speed up processing
- Improved addressing modes
- New instructions

# HC12 Programmer's Model



## Stack before/after IT



Note: Different from HC11 – SP points to last element pushed, NOT next empty slot

# HC12 New Addressing Modes

Indexed (5-bit offset)	<b>INST</b> <i>opr</i> x5, <i>xy</i> sp	IDX	5-bit signed constant offset from X, Y, SP, or PC
Indexed (pre-decrement)	<b>INST</b> <i>opr</i> x3,- <i>xy</i> s	IDX	Auto pre-decrement x, y, or sp by 1 ~ 8
Indexed (pre-increment)	<b>INST</b> <i>opr</i> x3,+ <i>xy</i> s	IDX	Auto pre-increment x, y, or sp by 1 ~ 8
Indexed (post-decrement)	<b>INST</b> <i>opr</i> x3, <i>xy</i> s-	IDX	Auto post-decrement x, y, or sp by 1 ~ 8
Indexed (post-increment)	<b>INST</b> <i>opr</i> x3, <i>xy</i> s+	IDX	Auto post-increment x, y, or sp by 1 ~ 8
Indexed (accumulator offset)	<b>INST</b> <i>abd</i> , <i>xy</i> sp	IDX	Indexed with 8-bit (A or B) or 16-bit (D) accumulator offset from X, Y, SP, or PC
Indexed (9-bit offset)	<b>INST</b> <i>opr</i> x9, <i>xy</i> sp	IDX1	9-bit signed constant offset from X, Y, SP, or PC (lower 8 bits of offset in one extension byte)
Indexed (16-bit offset)	<b>INST</b> <i>opr</i> x16, <i>xy</i> sp	IDX2	16-bit constant offset from X, Y, SP, or PC (16-bit offset in two extension bytes)
Indexed-Indirect (16-bit offset)	<b>INST</b> [ <i>opr</i> x16, <i>xy</i> sp]	[IDX2]	Pointer to operand is found at... 16-bit constant offset from X, Y, SP, or PC (16-bit offset in two extension bytes)
Indexed-Indirect (D accumulator offset)	<b>INST</b> [D, <i>xy</i> sp]	[D,IDX]	Pointer to operand is found at... X, Y, SP, or PC plus the value in D

# HC12 Addressing Modes

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- INH, IMM, DIR, EXT, REL as before
- Improved indexing:
  - » X, Y, SP(PC) can all be used
- IDX variants:
  - » Constant offset:
    - 5-bit signed constant offset, X/Y/SP/PC
    - 9-bit signed constant offset, X/Y/SP/PC
    - 16-bit constant offset, X/Y/SP/PC
  - » Accumulator offset:
    - A/B(8-bit) or D(16-bit) offset, X/Y/SP/PC

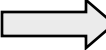
# HC12 Addressing Modes

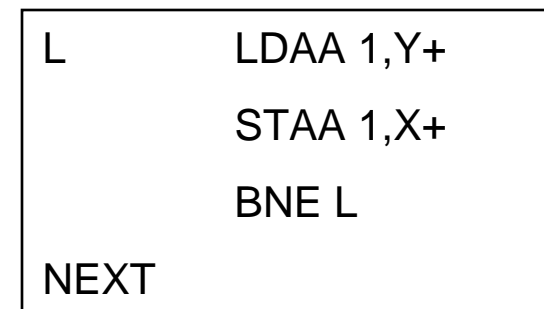
## Improved indexing

- » Automatic pre/post decrement/increment, X/Y/SP:
  - Pre: Before accessing data, Post: after accessing data
  - Increment/Decrement by 1~8

HC11	HC12
PSHA	STAA 1,-SP
PULA	LDAA 1,SP+
PSHX	STX 2,-SP
PULX	LDX 2,SP+

– Example:

- In C: `while(*x++ = *y++);` 



# HC12 Addressing Modes

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## Improved indexing

- Indexed-indirect

INST [opr<sub>x16</sub>,xy<sub>sp</sub>]

Pointer to operand is found  
at 16-bit constant offset from X/Y/SP/PC

- Indexed-indirect

INST [D,xy<sub>sp</sub>]

Pointer to operand is found at  
X/Y/SP/PC plus the value in D

Rationale for new addressing modes:

Better support for high-level languages/compiler

# New HC12 Instructions

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- Direct Memory-to-memory move

LOOP          MOVW 2,X+ , 2,Y+          Move word, incr. X/Y

                DBNE                  B,LOOP                  Repeat B times

- Universal transfer instruction

» Exchange between any two registers

- Loop constructs:

– Decrement/Increment/Test counter, then branch on zero/non-zero: D/I/T BNE/BEQ

- Minimum/maximum instructions:

– MINA op: set A to min of (A,op) - also MAXA

– MINM op: set M to min of (A,M) - also MAXM

# New HC12 Instructions

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- Fuzzy Logic Instructions
  - » Special instructions for fuzzy logic calculations
- Table lookup instructions: TBL, ETBL
  - » Linear interpolation in tables with 8/16 bit values
  - » B: fractional value (<1!), opr: points to y1
  - »  $\text{Result} = y1 + B * (y2 - y1)$
- Bit manipulations instructions work in direct/extended/indexed addressing modes
- Push/pull D and CCR (3 bytes)
- Compare SP value

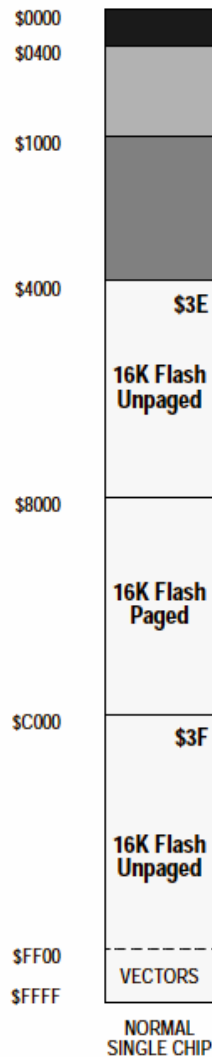
For details, see:

[CPU12 Reference Guide](#)

[Transporting MC68HC11 Code to MC68HC12 Devices](#)

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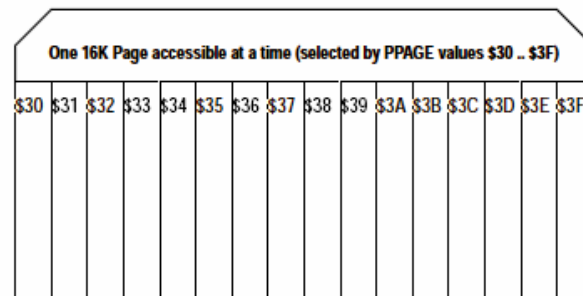
# Paged Memory in HC12



Registers: I/O, control, etc.

EEPROM

RAM



9S12DP256 has 256kbytes of flash memory on chip.

It is divided into 16x16 kbyte pages, which are accessible at \$8000.

Which actual page from the 16 is active, is determined by a *page register*: PPAGE

CPU still uses 16-bit addresses. If you want to use pages, the PPAGE register must be explicitly manipulated.

Special instructions:

CALL addr,page

RTC