EECE 276
Embedded Systems

HC 12 Overview: Interface devices
ICE/LAN debugging tools

HC12 Interfaces

- 9S12DP256: Complex HC12 system
  - » HC12 here means: 9S12DP256
- On-chip memory
  - » EEPROM (4K)
  - » RAM (12K)
  - » Flash (256K)- tricky to access
- Various operating modes (see ref. guide)

HC12 Interfaces

- Enhance Capture Timer
  - » Similar to HC11 timer unit:
    - – Input capture, output compare, pulse accumulator
- Serial Communication Interface
  - » DUART – Asynchronous (w/o clock line)
- Serial Peripheral Interface
  - » Synchronous, serial port
- Inter-IC Bus
  - » 2-wire, bidirectional serial bus (100KBPS)

HC12 Interfaces

- Motorola Scalable Controller Area Network (CAN)
  - » CAN is a serial bus/protocol, widely used in automotive manufacturing
  - » Data rates up to 1Mbps
  - » MSCAN is an implementation of it
- Analog to Digital Converter
  - » 8/10 bit S/A converter
- Byte Data Link module
  - » SAE J1850 serial communication protocol
- BDM: Background Debug Module
  - » HW Support for debugging another device (aka mini-ICE)
- BKP: Breakpoint Module
  - » HW support for breakpoints

Development tools: LAN

Logic Analyzer

- Multi-channel digital scope
- Connected to the bus signals of a micro system
- Samples and stores signal state in memory
- Logic analysis:
  - *Timing* analysis: sampling signals according to an external (asynchronous) clock
  - *State* analysis: sampling is triggered by an internal event (e.g. E-clock on 68HC11)
- Display:
  - Timing diagram, Hex address/data, Instructions

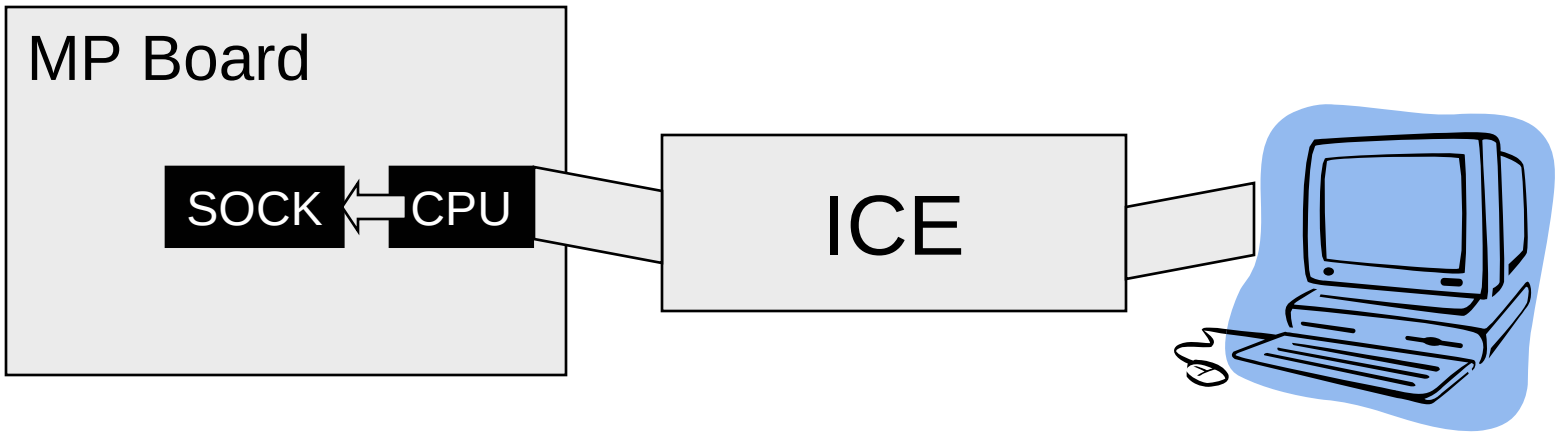
Development tools: LAN

Logic Analyzer

- » HP 1650A: 80 channels, 100 MSamples/sec, 1kbit/channel storage
- » Qualification/triggering: Sample only when needed
  - – When a certain combination appears on Address/Data bus lines (‘don’t-care’-s allowed)
  - – Trigger based on previous or simultaneous events
  - – Chained conditions (“sequence levels”)
  - – Prestore: (e.g. store instructions to determine which has modified a memory location)
  - – Cross triggering:
    - State analysis – triggers-> Timing analysis

Development tools: ICE

In-Circuit Emulator



CPU Hardware Emulator

- » It *emulates* in HW what the CPU is doing
- » PC is used to control the emulation process

Development tools: ICE

MetaLink ICE Services:

- Define/configure memory (address, size, type)
- Download program, take snapshot of memory
- Execute code, control code execution
- Breakpoints on:
  - Code, write access, write protect violation
- Trace buffer: stores executed instructions
- Search for frames in Trace Buffer
- Complex breakpoints:
  - Logic functions over address (bits), opcode values, etc.
- Symbolic debugging support (ASM, C)
- Performance analyzer:
  - Where does the program spend its time?
- Raw data on signals (waveforms)
- Direct manipulation of CPU registers