EECE 218
Microcontrollers

Bus electronics
Bus electronics

- Industry standard buses: standardized methods for interconnecting components
- They carry:
  » address/data/control signals + power
- Examples:
  » ISA: 16-bit bus for PC-s
  » PCI: 32-bit bus for PC-s
  » VME: 32-bit bus for industrial controllers
- Standards have 3 layers:
  » Mechanical (dimensions, forces, etc.)
  » Electrical (voltage/current levels)
  » Logical (protocol)
Interfacing issues

- Fan-in/fan-out: # of drivers/# of receivers
  - One driver must be able to drive >N receivers
- High-speed design: Delays/reflection
  - Bus termination
- Different types of devices:
  - There are many different digital logic device technologies: TTL, HCMOS, NMOS, CMOS, ECL…
  - Issues:
    - Current matching: driver must be able to source/sink sufficient current for all the receivers connected to it.
    - Voltage level matching…
Interfacing issues

- Driver/receiver combination:

![Diagram of driver/receiver combination with tables and graphs showing voltage levels and currents for different logic families.](image)
Interfacing issues

- Noise immunity: the gate’s noise suppression (signal recovery) capability
- Well-designed system:
  - Noise margins

\[ V_{OH} \quad V_{IH} \quad V_{IL} \quad V_{OL} \]

\[ V_{HNM} \quad V_{LNM} \]
Interfacing issues

When mixing technologies noise margins must be positive!

Noise margins:

<table>
<thead>
<tr>
<th>Output Logic</th>
<th>LS TTL</th>
<th>S TTL</th>
<th>ALS TTL</th>
<th>NMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LS TTL</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>1.0/−0.8</td>
</tr>
<tr>
<td>S TTL</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>0.3/0.7</td>
<td>1.0/−0.8</td>
</tr>
<tr>
<td>ALS TTL</td>
<td>0.4/0.7</td>
<td>0.4/0.7</td>
<td>0.4/0.7</td>
<td>0.4/0.7</td>
<td>1.1/−0.8</td>
</tr>
<tr>
<td>NMOS</td>
<td>0.4/0.4</td>
<td>0.4/0.4</td>
<td>0.4/0.4</td>
<td>0.4/0.4</td>
<td>1.1/−1.0</td>
</tr>
<tr>
<td>CMOS</td>
<td>0.79/2.99</td>
<td>0.79/2.99</td>
<td>0.79/2.99</td>
<td>0.79/2.99</td>
<td>1.45/1.45</td>
</tr>
</tbody>
</table>

Note: Each value is presented as “logical 0/logical 1” noise immunity. The effective value is the lower of this pair.
Interfacing issues

- Multiple drivers on the same line:

  Short circuit to the GND!

  The outputs of simple logic gates cannot be connected.
Multiple drivers

Signals driven by multiple drivers

Open-collector design

- Pull-up resistor
- Chip1: {L,-}
- Chip2: {L,-}
- Chip3

Open Collector drivers

Implements wired-OR logic

Tri-state design

- SEL1 AND SEL2 = FALSE
- Chip1: {H,L,Z}
- Chip2: {H,L,Z}
- Chip3

Tri-state drivers

Drivers are independent
Comparison

<table>
<thead>
<tr>
<th>Open collector</th>
<th>Tri-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mixes signals</td>
<td>Signals independent</td>
</tr>
<tr>
<td>Needs pullup R</td>
<td>Needs control signal</td>
</tr>
<tr>
<td>Safe</td>
<td>Wrong control -&gt; smoke</td>
</tr>
<tr>
<td>High V/I</td>
<td>Normal V/I</td>
</tr>
</tbody>
</table>

Applications:

- IRQ line
  - Any IO devices can activate -IRQ