EECE 276
Embedded Systems

Refresh of basic HW concepts, HW interfacing
HW Concepts

- Combinational circuits – Boolean logic
  - Basic gates: NOT, AND, OR
  - Complex circuits: multiplexers, FPGAs, etc.

- Sequential circuits
  - Synchronous – clock-driven
  - State/memory: (D) flip-flops
  - Moore/Mealy models

- Von-Neumann Machine
  - Instruction Set Arch.
Hardware concepts

Basic architecture

CPU | Memory | I/O

Bus: Address, Data, Control

Microcontrollers: On-chip memory and (specialized) I/O interface circuits
HW Interfacing Concepts

Latching:
“Recording” the appearance of a signal for later processing. (Think about D flip-flop). Once data is latched, it stays there until the latch is cleared.

Edge-triggered vs. level triggered:
E/T: fast change in signal indicates an event
• Falling/rising edge -> trigger
L/T: a signal crossing a (value) threshold indicates an event.
• Once signal crosses threshold, data is latched.
HW Interfacing Concepts

Edge-triggered

Level-triggered

Trigger

Trigger

Trigger

Trigger

Trigger
HW Interfacing Concepts

Signals driven by multiple drivers

Open-collector design

- Chip1
- Chip2
- Chip3

Open Collector drivers

Implements wired-OR logic

Pull-up resistor

Tri-state design

- Chip1
- Chip2
- Chip3

Tri-state drivers

Drivers are independent

SEL1 AND SEL2 = FALSE

SEL1

SEL2

{H,L,Z}

{H,L,Z}

{L,-}

{L,-}
Hardware Concepts

**Buses**

*Goal:* to interconnect devices through a shared physical medium

*Typical system bus:* CPU, Memory, I/O connected via Address/Data/Control/Power lines.

*I/O Device connection buses:*

- PCI: high-speed parallel, system bus
- SCSI: high-speed parallel, daisy-chained bus
- MIL-STD-1553B: master/slave serial bus
- IEEE-1394 (Firewire): high-speed serial bus with support for asynchronous and streaming (isochronous) transfers
- USB: high-speed serial bus with hub-and-spoke architecture