FPGA Design
EECE 277
Examples of Digital System Design

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March 4, 2005

http://eecs.vanderbilt.edu/courses/eece277/

Topics
“And now for something completely different.”
– Monty Python’s Flying Circus

• Administrative stuff
  – Web site access
  – Read Chapter 10 in your textbook
  – Homework Assignment #4 (due Wednesday, March 16)

• Algorithmic State Machine (ASM) chart
• Datapath
• Control

Algorithmic State Machine (ASM) Chart

• Implicitly specifies that FSM changes state only after each clock edge

Example: Moore Type

State table

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state $w = 0$</th>
<th>Output $z$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>A</td>
<td>1</td>
</tr>
</tbody>
</table>

Example: Mealy Type

State table

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Output z</th>
</tr>
</thead>
<tbody>
<tr>
<td>w = 0</td>
<td>w = 1</td>
<td>w = 0</td>
</tr>
<tr>
<td>A A</td>
<td>B 0</td>
<td>0</td>
</tr>
<tr>
<td>B A</td>
<td>B 0</td>
<td>1</td>
</tr>
</tbody>
</table>

General Model for Sequential Circuits

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Example: Multiplication

The Big Picture

- Since 1946 (ENIAC I) all computers have had 5 components

- What pattern do you see for binary multiplication?
ASM Chart for Multiplier

What control signals are necessary for this datapath?

(b) Pseudo-code

P = 0;
for i = 0 to n - 1 do
  if b_i = 1 then
    P = P + A;
  end if;
  left-shift A;
end for;

Datapath for Multiplier
Basic Instruction Cycle

- **Fetch**
  - Get the next instruction from memory

- **Decode**
  - Determine which instruction to perform

- **Execute**
  - Perform the instruction

Summary

- A digital system consists of two main parts, the datapath circuit and the control circuit.

- Algorithmic State Machine (ASM) charts can be used to describe these larger systems.

- The basic state machine sequence for a processor is *fetch-decode-execute*. 