FPGA Design
EECE 277

Implementation Technology

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http://eecs.vanderbilt.edu/courses/eece277/

Topics

“If at first you don’t succeed, try, try again.”
– Thomas H. Palmer (1782 - 1861)

• Administrative stuff
  – Homework #2 Assigned (Chapter 3)
  – UP2 Kits and lab partners
  – Complete tutorials in Appendices B, C, and D
  – Collect Homework #1

• Transistors
• Integrated circuits
• Programming technology

Technology Timeline


- Transistors
- ICs (General)
- SRAMs & DRAMs
- Microprocessors
- CPLDs
- ASICs
- FPGAs

- White bar represents technology introduction
- Gray bar represents widespread use

Translating Voltage Levels

- $V_{1,\text{min}}$ represents lowest voltage still counted as logic ‘1’
- $V_{0,\text{max}}$ represents highest voltage still counted as logic ‘0’

$V_D$ (Gnd)

Logic value 1

Undefiend

Logic value 0

$V_{DD}$

Fundamentals of Digital Logic
Chapter 3
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**NMOS Transistors**

- Turned on when gate terminal is high
- When on, drain is pulled down to GND
- Cannot be used to pull drain completely up to \( V_{DD} \)

\[ V_G = 0 \text{ V} \]
\[ V_D = 0 \text{ V} \]

Closed switch when \( V_G = V_{DD} \)
Open switch when \( V_G = 0 \text{ V} \)

**PMOS Transistors**

- Turned on when gate terminal is low
- When on, drain is pulled up to \( V_{DD} \)
- Cannot be used to pull drain completely down to GND

\[ V_G = V_{DD} \]
\[ V_D = 0 \text{ V} \]

Open switch when \( V_G = V_{DD} \)
Closed switch when \( V_G = 0 \text{ V} \)

**CMOS Logic Gates**

- **Pull-up network**: PMOS transistors
- **Pull-down network**: NMOS transistors

**In CMOS Logic Gates**

- Current flows more readily in NMOS transistors than PMOS transistors
- For transistors of equal size, an NMOS transistor has a current capacity 2x – 3x greater than a PMOS
- For equal pull-up/pull-down characteristics, PMOS transistors are sized 2x – 3x larger than NMOS transistors
(a) Circuit

(b) Truth table and transistor states

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CMOS NAND Gate

(a) Circuit

(b) Truth table and transistor states

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CMOS NOR Gate

(a) Circuit

(b) Truth table and transistor states

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7400 Series Chip

(a) Dual-inline package

(b) Structure of 7404 chip
Using TTL Chips for Logic Functions

Figure 3.22. An implementation of $f = x_1x_2 + x_2x_3$.

Integration Levels

- **Small Scale Integration (SSI)**
  - One to ten devices

- **Medium Scale Integration (MSI)**
  - Ten to 100 devices

- **Large Scale Integration (LSI)**
  - 100 to 100,000 devices

- **Very Large Scale Integration (VLSI)**
  - Greater than 100,000 devices

Random Access Memory (RAM)

- **Static RAM (SRAM)**
  - Constructed from circuits similar to D flip-flop
  - Contents retained while power is on
  - Used in Level 2 cache because of fast access times

- **Dynamic RAM (DRAM)**
  - Constructed with a transistor and capacitor
  - Contents must be "refreshed" due to charge leakage
  - Used in main memory because of high density

The Need for More Integration

We need to combine gates to provide a useful function that requires a limited number of external connections (pins).

- Using SSI, 5 million NAND gates would require 15,000,002 pins
- Infeasible for pin spacing requirements
Static RAM (SRAM)

- Six transistors in cross-connected fashion
  - Provides regular AND inverted outputs
  - Implemented in CMOS process

Dynamic RAM (DRAM)

- SRAM cells exhibit high speed/poor density
- DRAM: simple transistor/capacitor pairs in high density form

Technology Trends: Microprocessor Capacity

- Die size: 2X every 3 yrs
- Line width: halve / 7 yrs

Programmable Logic Devices (PLDs)

- General-purpose chip for implementing logic circuitry
- Customizable “black box” with gates and switches
**Taxonomy**

- **PLDs**
  - SPLDs
  - CPLDs
- **PROMs**
- **PLAs**
- **PALs**
- **GALs**
- **etc.**

**Acronyms**

- **SPLD** – Simple PLD
- **CPLD** – Complex PLD
- **PROM** – Programmable Read-Only Memory
- **PLA** – Programmable Logic Array
- **PAL** – Programmable Array Logic
- **GAL** – Generic Array Logic

**Adding “Programmable” in FPGA**

- Potential links
- Logic 1
- Pull-up resistors
- a \( \overline{\text{NOT}} \) \( \overline{\text{AND}} \) \( y = 1 \) (N/A)
- b \( \overline{\text{NOT}} \)

**Unprogrammed Fusible Links**

- Device manufactured with all links in programmable path (short circuit)
- Logic 1
- Pull-up resistors
- a \( F_{\text{fus}} \) \( \overline{\text{NOT}} \) \( \overline{\text{AND}} \) \( y = 0 \) (N/A)
- b \( F_{\text{fus}} \) \( \overline{\text{NOT}} \)
Programmed Fusible Links

- Disconnected fuses act as open circuits
- One-Time Programmable (OTP)

\[ y = a \lor !b \]

Pull-up resistors

\[ \text{Logic 1} \]

Unprogrammed Antifuse Links

- Device manufactured with high resistance in configurable path (open circuit)

\[ y = 1 \text{(N/A)} \]

Programmed Antifuse Links

- Connections are “grown”
- One-Time Programmable (OTP)

\[ y = !a \lor b \]

Growing an Antifuse

(a) Before programming

(b) After programming
Erasable PROM (EPROM)

- Requires ultraviolet (UV) radiation to remove stored charge on floating gates

Electrically Erasable PROM (E²PROM)

- Second transistor used to electrically erase the cell

Programming Technologies

<table>
<thead>
<tr>
<th>Technology</th>
<th>Symbol</th>
<th>Predominantly associated with ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fusible-link</td>
<td>- (\text{--}) -</td>
<td>SPLDs</td>
</tr>
<tr>
<td>Antifuse</td>
<td>-O----</td>
<td>FPGAs</td>
</tr>
<tr>
<td>EPROM</td>
<td>-[]</td>
<td>SPLDs and CPLDs</td>
</tr>
<tr>
<td>E²PROM/FLASH</td>
<td>-[]</td>
<td>SPLDs and CPLDs (some FPGAs)</td>
</tr>
<tr>
<td>SRAM</td>
<td>(\text{RAM})</td>
<td>FPGAs (some CPLDs)</td>
</tr>
</tbody>
</table>

Programmable Read-Only Memory (PROM)

- Fixed AND array with programmable OR array
Programmable Logic Array (PLA)

- Both AND array and OR array are programmable

![Programmable Logic Array Diagram](image)

Slower device because signals pass through programmed links

Programmable Array Logic (PAL)

- Programmable AND array with fixed OR array

![Programmable Array Logic Diagram](image)

Complex Programmable Logic Device (CPLD)

- PAL-like block
- Interconnection wires
- I/O block

Summary

- VLSI technology allows more functionality to be incorporated on a single chip
- CMOS circuits use pull-up networks (PMOS) to pass logic ‘1’ and pull-down networks (NMOS) to pass logic ‘0’
- FPGAs typically use either antifuse or SRAM technology for configuration