FPGA Design
EECE 277

Interconnect and Logic Elements

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http://eecs.vanderbilt.edu/courses/eece277/

Topics
“i don’t know their names. can i give you their numbers?”
– Freddy Mitchell
WR for the Philadelphia Eagles

• Administrative stuff
  – Homework Assignment #2 (due Wednesday, February 2)
  – Laboratory Assignment #1 (due Friday, February 4)
• FPGA review
• Interconnect issues
• Logic element issues

Guest Lecture

• Dr. Robinson will be on travel
  – Friday, January 28, 2005

• Presentations on current FPGA research
  – Jason Scott
    • Embedded System Design Tools and Xilinx FPGAs
  – Philippe Adell
    • Implementing a Rad-Hard digital power controller with an FPGA

Potential Final Project Ideas!!!

Laboratory Assignment #1

• Quartus II Software
  – Any installation issues?
• UP2 Design Laboratory Kits
  – Any configuration issues?
• Laboratory Report
  – Follow guidelines from handout
• Potential Lab Session
  – Tuesday, cancelled
  – Wednesday during normal class time
FPGA Fabric (Architecture)

- Logic
- Interconnect
- I/O pins

FPGA Fabric Questions

- Given limited area budget
  - How many logic elements?
  - How much interconnect?
  - How many I/O blocks?

Logic Element Questions

- How many inputs?
- How many functions?
  - All functions of \( n \) inputs or eliminate some combinations?
  - What inputs go to what pieces of the function?
- Any specialized logic?
  - Adder, etc.
- What register features?

Interconnect Questions

- How many wires in each channel?
- Uniform distribution of wiring?
- How should wires be segmented?
- How rich is interconnect between channels?
- How long is the average wire?
- How much buffering do we add to wires?
I/O Block Questions

- How many pins?
  - Maximum number of pins determined by package type.
- Are pins programmed individually or in groups?
- Can all pins perform all functions?
- How many logic families do we support?

Programming Technologies

- What types are available?

<table>
<thead>
<tr>
<th>Technology</th>
<th>Symbol</th>
<th>Predominantly associated with ...</th>
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</thead>
<tbody>
<tr>
<td>Fusible-link</td>
<td></td>
<td>SPLDs</td>
</tr>
<tr>
<td>Antifuse</td>
<td>![Antifuse Symbol]</td>
<td>FPGAs</td>
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<tr>
<td>EPROM</td>
<td>![EPROM Symbol]</td>
<td>SPLDs and CPLDs</td>
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<td>E²PROM/FLASH</td>
<td>![E²PROM Symbol]</td>
<td>SPLDs and CPLDs (some FPGAs)</td>
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<tr>
<td>SRAM</td>
<td>![SRAM Symbol]</td>
<td>FPGAs (some CPLDs)</td>
</tr>
</tbody>
</table>

SRAM-Based FPGAs

- Program logic functions, interconnect using SRAM
- Advantages:
  - Re-programmable
  - Dynamically reconfigurable
  - Uses standard processes
- Disadvantages:
  - SRAM burns power
  - Possible to steal, disrupt configuration bits

Terminology

- Configuration:
  - Bits that determine logic function + interconnect
- CLB:
  - Combinational Logic Block = Logic Element (LE)
- LUT:
  - Lookup table = SRAM used for truth table
- I/O block (IOB):
  - I/O pin + associated logic and electronics
Example: FPGA Configuration

• Your FPGA has 9 logic elements (LE) each with four inputs and one output

• There are four vertical and four horizontal routing channels with four wires per channel

• Each wire in the routing channel can be connected to every input of the LE on its right and the output of the LE on its left

• When two routing channels intersect, all possible connections between the intersecting wires can be made

• How many configuration bits are required?

Configuration

• Must set control bits for
  – LE
  – Interconnect
  – I/O blocks

• Usually configured off-line
  – Separate burn-in step (antifuse)
  – At power-up (SRAM)

Example: FPGA Configuration

• How many configuration bits are required?

580 configuration bits

– LE SRAMs: $16 \times 9 = 144$
– I/O connections of LEs: $20 \times 9 = 180$
– Routing channel intersections: $16 \times 16 = 256$

Programmable Interconnection Point

Figure 3.68. Pass-transistor switches in FPGAs.
Programmable vs. Fixed Interconnect

- Switch adds delay
- Transistor off-state is worse in advanced technologies
- FPGA interconnect has extra length
  - Equals added capacitance

Interconnect Strategies

- Some wires will not be utilized
- Congestion will not be same throughout chip
- Types of wires
  - Short wires: local LE connections
  - Global wires: long-distance, buffered communication
  - Special wires: clocks, etc.

Paths in Interconnect

- Connection may be long and complex

Interconnect Architecture

- Connections from wiring channels to LEs
- Connections between wires in the wiring channels
Interconnect Richness

- **Within a channel:**
  - How many wires
  - Length of segments
  - Connections from LE to channel

- **Between channels:**
  - Number of connections between channels
  - Channel structure

Segmented Wiring

Channel Intersections (Switchbox)

Interconnect paths
Logic Element (LE) Output Drivers

- Must drive load
  - Wire
  - Destination LE

- Different types of wiring present different loads

Interconnect Circuits

- Why so many types of interconnect?
  - Provide a choice of delay alternatives.

- Sources of delay
  - Wires
  - Programming points

Styles of Programmable Interconnection Points

- Pass transistor
- Three-state

Using a Pass Transistor

- Small area.
- Resistive switch.
- Delay grows as the square of the number of switches.
Using a Three-State Buffer

- Larger area.
- Regenerative driver.

Evaluation of SRAM-based LUT

- N-input LUT can handle function of $2^n$ input combinations
- All logic functions take the same amount of space
- All functions have the same delay
- SRAM is larger than static gate equivalent of function
- Burns power at idle

FPGA Fabric (Architecture)

- Logic
- Interconnect
- I/O pins

Summary

- Regular placement of logic elements leads to regular structure of interconnect
- Delays are affected by path length and the switching points
- Logic elements are used to implement functions