Analog Devices
ADSP-2106x SHARC

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There are 10 types of people in the world: people who understand binary, and people who have friends.
Why use a DSP?

- Fast filtering operations
- High-bandwidth communications
- Specialized embedded applications
- Reduce load on general-purpose CPU
What is the SHARC?

- Super Harvard Architecture Computer
- 32-bit DSP
- IEEE Floating-Point Computation Units
- Many External ports
The SHARC meets five central DSP requirements

- Fast, flexible arithmetic computation units
- Extended precision in the computation units
- Unconstrained data flow to and from computation units
- Dual address generators
- Efficient program sequencing

From the ADSP-2106x User’s Manual
Fast, flexible computation units avoid structural stalls

- All instructions execute in one cycle
- IEEE floating-point compatible
- Independent computational units increase ILP
Extended-precision computational units limit intermediate truncation errors

- 40-bit data register file
- 64-bit fixed-point product register with 80-bit accumulator
- Extended-precision 40-bit IEEE floating point format
Unconstrained data flow is essential for efficient operation

- 10-port data register file
- 48-bit instruction word for ILP
- Super Harvard Architecture
- In one cycle:
  - Read/write 2 operands to data register file
  - Supply 2 operands to CPU
  - Supply 2 operands to multiplier
  - Receive 2 results from ALU/multiplier
Dual address generators and efficient program sequencing streamline operation

- Dual **Data Address Generators** free up computational units
- Each DAG keeps 8 address pointers, 8 modifiers, and 8 length values
- Circular buffers improve filtering performance and Fourier transforms
- Program sequencer controls looping and branching
- Pipelined *fetch, decode, execute*
- 6 levels of zero-overhead looping
SHARC overview

- Separate data and memory buses
- Separate I/O processor with dedicated buses
- More parallelism than Von Neumann architecture
Architecture overview
Analog Devices SHARC trends

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<th>Generation</th>
<th>Clock/ MFLOPs</th>
<th>Features</th>
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<td>First</td>
<td>66 MHz</td>
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<td>198 MFLOPs</td>
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<td>Second</td>
<td>100 MHz</td>
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<td>600 MFLOPs</td>
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<td>Third</td>
<td>300 MHz</td>
<td>Dual cores</td>
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<td>1800 MFLOPs</td>
<td>On-chip memory</td>
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* Single Instruction, Multiple Data
Sources

- ADSP-2106x User’s Manual
- BDTI (Berkeley Design Technology, Inc.)
  http://www.bdti.com/procsum/adi060.htm