Topics

• Reminders
  – Homework due this Friday (10-10)
  – Exam 2 on next Friday (10-17)

• ALU Design

• Memory

• CPU chips and buses

Datapath of IJVM

• Microarchitecture (Level 1)
  – Formed using digital logic (level 0)
  – Includes decoders, adders, registers, etc.
Control Signals for ALU Functions

<table>
<thead>
<tr>
<th>$F_2$</th>
<th>$F_1$</th>
<th>ENA</th>
<th>ENB</th>
<th>INVA</th>
<th>INC</th>
<th>Function</th>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>B</td>
</tr>
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<td>1</td>
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<td>1</td>
<td>0</td>
<td>A</td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>A + B</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>A + B + 1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>A + 1</td>
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<tr>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>B + 1</td>
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<td>1</td>
<td>0</td>
<td>B - A</td>
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<tr>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>B - 1</td>
</tr>
<tr>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-A</td>
</tr>
<tr>
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<td>0</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>A AND B</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1 - 1</td>
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</table>

*Figure 4-2. Useful combinations of ALU signals and the function performed.*
Combining Bit Slices for ALU

Set Reset (SR) Latch

- Contains cross-coupled gates to remember state
- $R = S = 0$ causes the latch to “hold” its current value
- $S = 1$ (while $R = 0$) sets $Q$ to 1
- $R = 1$ (while $S = 0$) resets $Q$ to 0
- $R = S = 1$ causes instability in the latch
Clocked SR Latch

- Useful to prevent latch from changing state except at certain times
- Add **AND** gates to enable S and R on clock high
- What about \( R = S = 1 \)?
  - causes instability on cross-coupled NOR gates when clock is high

Clocked Data (D) Latch

- Resolve SR instability by preventing it from occurring
- Use one input (D) for the latch
- True 1-bit memory
**D Flip-Flop**

- Difference between flip-flop and latch
  - A flip-flop is edge triggered
  - A latch is level triggered

**Registers**

- D flip-flops combined to operate as a group
- Forms an 8-bit register (1 byte)
- Use additional chips in parallel for larger registers
Memory Organization

- Input bits for memory write
- 2:4 Decoder using address lines
- Chip Select Read Output Enable
- Output bits for memory read using non-inverting buffer

Memory Chips

- Regular memory structure allows extension to larger sizes
  - Add rows (and associated connections) to increase number of words
  - Add columns (and associated connections) to increase number of bits per word

- Terminology
  - Asserted – signal set to cause some action
  - Negated – signal not set for an action
Random Access Memory (RAM)

- **Static RAM (SRAM)**
  - Constructed from circuits similar to D flip-flop
  - Contents retained while power is on
  - Used in level 2 cache because of fast access times

- **Dynamic RAM (DRAM)**
  - Constructed with a transistor and capacitor
  - Contents must be “refreshed” due to charge leakage
  - Used in main memory because of high density

Read-Only Memory (ROM)

- **Programmable ROM (PROM)**
  - Programmed once using fuses

- **Erasable PROM (EPROM)**
  - Can be reused after erasing with UV light

- **Electrically Erasable PROM (EEPROM)**
  - Electrical pulses on special input pin erases device
  - Flash memory is a type of EEPROM that is block erasable
Comparison of Memory Types

<table>
<thead>
<tr>
<th>Type</th>
<th>Category</th>
<th>Erasure</th>
<th>Byte alterable</th>
<th>Volatile</th>
<th>Typical use</th>
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<tr>
<td>SRAM</td>
<td>Read/write</td>
<td>Electrical</td>
<td>Yes</td>
<td>Yes</td>
<td>Level 2 cache</td>
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<tr>
<td>DRAM</td>
<td>Read/write</td>
<td>Electrical</td>
<td>Yes</td>
<td>Yes</td>
<td>Main memory</td>
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<td>ROM</td>
<td>Read-only</td>
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<td>No</td>
<td>No</td>
<td>Large volume appliances</td>
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<tr>
<td>PROM</td>
<td>Read-only</td>
<td>Not possible</td>
<td>No</td>
<td>No</td>
<td>Small volume equipment</td>
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<tr>
<td>EPROM</td>
<td>Read-mostly</td>
<td>UV light</td>
<td>No</td>
<td>No</td>
<td>Device prototyping</td>
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<tr>
<td>EEPROM</td>
<td>Read-mostly</td>
<td>Electrical</td>
<td>Yes</td>
<td>No</td>
<td>Device prototyping</td>
</tr>
<tr>
<td>Flash</td>
<td>Read/write</td>
<td>Electrical</td>
<td>No</td>
<td>No</td>
<td>Film for digital camera</td>
</tr>
</tbody>
</table>

Computer Buses

- **Bus** – common electrical pathway between multiple devices
Bus Clocking

- **Synchronous**
  - Uses master clock driven by crystal oscillator
  - All transactions occur as multiples of “bus cycles”
  - Timing diagram defines the bus protocol *(Fig 3-37)*

- **Asynchronous**
  - Does not require a master clock
  - Transactions can use any length required
  - Full handshake defines the bus protocol *(Fig 3-38)*

**Bus Arbitration**

*Figure 3-39.* (a) A centralized one-level bus arbiter using daisy chaining. (b) The same arbiter, but with two levels.
Example Buses

- **Industry Standard Architecture (ISA)**
  - Found in every Intel-based PC
  - Maximum bandwidth of 16.7 MB/sec

- **Peripheral Component Interconnect (PCI)**
  - Patents in public domain to encourage third-party use
  - Maximum bandwidth of 528 MB/sec

- **Universal Serial Bus (USB)**
  - Industry consortium design for low-speed I/O devices
  - Bus protocol similar to network with data packets contained in frames
  - Maximum bandwidth of 1.5 MB/sec

Pentium II System Architecture

Uses multiple buses with bridges to connect them