Wednesday, September 22, 2004

SOLUTIONS!!!

Name (print): ____________________________________________________________

Signed: __________________________________________________________________

_I pledge my honor that I have neither given nor received aid on this work._

GENERAL INSTRUCTIONS

1. Do not open this exam until instructed to do so.

2. This is a **closed book, closed notes** exam. Use a pencil to complete your work. Follow the instructions as given in the problem. Calculators **ARE NOT** allowed for the exam.

3. Please do all of your work on the exam itself. You may use the backs of the pages, if necessary. Clearly indicate the continuation of your work on other pages.

4. Show work for maximum partial credit.

5. Please be as neat and as well-organized as possible.

6. Clearly indicate your answers.

<table>
<thead>
<tr>
<th></th>
<th>MAXIMUM</th>
<th>SCORE</th>
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<tr>
<td>TOTAL</td>
<td>100</td>
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</table>
1. Label the following two architectures based upon their memory structure. (4 pts)

Harvard architecture

von Neumann architecture

2. List the three levels of parallelism used to improve computer performance. (3 pts)

- Data-Level Parallelism (DLP)
- Instruction-Level Parallelism (ILP)
- Thread-Level Parallelism (TLP)

3. The VandyDore microarchitecture uses a two-way set associative instruction cache with a size of 128 KB. The microarchitecture has a 32-bit datapath. Each cache line holds 32 bytes. Partition and label the following address bits into the four components used to store and retrieve data from the cache. (10 pts)
4. The first generation of computers was characterized by the use of vacuum tubes. Name the following machines from that era. (6 pts)

ENIAC  This machine is regarded as the beginning of the modern computer age.

COLOSSUS  This machine is the world’s first electronic digital computer.

IAS machine  This machine was built at Princeton by computer pioneer John von Neumann.

5. Answer the following questions regarding basic coding theory: (4 pts)

a) What is the minimum distance required for a binary code that can correct all double errors?

\[ 2 \leq \frac{1}{2} \times (d_{\text{min}} - 1) \]

\[ d_{\text{min}} = 5 \]

b) If the code from part (a) is used only to detect errors, what is the maximum number of errors guaranteed to be detected?

\[ \text{number of errors} \leq (d_{\text{min}} - 1) \]

Maximum number of errors = 4

6. The textbook describes a structured computer organization with six levels. Name each level in the correct order with Level 0 representing the lowest level and Level 5 representing the highest level. (6 pts)

Level 5  Problem-oriented language level

Level 4  Assembly language level

Level 3  Operating system machine level

Level 2  Instruction set architecture level

Level 1  Microarchitecture level

Level 0  Digital logic level
7. A computer has a three-level cache. Suppose that 70% of the memory references hit on the first level cache, 10% hit on the second level cache, 10% on the third level cache, and 10% miss (i.e. must access main memory). The access times are 5ns, 15ns, 20ns, and 60ns respectively. Access times for levels beyond the first cache start counting at the moment it is known that they are needed. What is the average access time? (4 pts)

\[
\text{AMAT} = 0.7 \times (5)\text{ns} + 0.1 \times (5+15)\text{ns} + 0.1 \times (5+15+20)\text{ns} + 0.1 \times (5+15+20+60)\text{ns}
\]
\[
\text{AMAT} = 3.5\text{ns} + 2\text{ns} + 4\text{ns} + 10\text{ns}
\]
\[
\text{AMAT} = 19.5 \text{ ns}
\]

8. List and define three types of cache misses. (9 pts)

- **Compulsory** – cache is empty at the start of a program

- **Conflict** – another valid cache line is currently stored in the location

- **Capacity** – cache isn’t large enough to hold the entire working set of a program

9. Data can be transmitted across regular phone lines using a modem. The data is encoded using a modulated sine wave. For each figure, name the type of modulation used to encode the given bit stream (6 pts)

   a. Frequency modulation

   b. Phase modulation

   c. Amplitude modulation

(a) 
(b) 
(c)
10. Using the following list of memory references, give the final state of the direct-mapped cache. The cache contains 16 lines. Assume the architecture has a 16-bit datapath. Also, each cache line holds 32 words. Place your hexadecimal answers appropriately in the table below. (10 pts)

Address read 1: 0x974C
Address read 2: 0xD9D6
Address read 3: 0x9776
Address read 4: 0x71E2

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<th>Tag</th>
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<tr>
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<tr>
<td>1</td>
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</tr>
<tr>
<td>2</td>
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<tr>
<td>4</td>
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<tr>
<td>5</td>
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</tr>
<tr>
<td>6</td>
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<td></td>
</tr>
<tr>
<td>7</td>
<td>Y</td>
<td>0x1C</td>
</tr>
<tr>
<td>8</td>
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<td></td>
</tr>
<tr>
<td>9</td>
<td>N</td>
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<tr>
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<td>12</td>
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<tr>
<td>13</td>
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<td>0x25</td>
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<tr>
<td>14</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>N</td>
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</tbody>
</table>

11. For the IEEE Floating Point Standard 754, how many total bits are used for extended precision within floating point units? (2 pts)

   Extended precision contains 80 bits
12. Computer architecture designers do their best to follow the RISC design principles. Write “RISC” next to each of the following which are included in the textbook as RISC design principles. (10 pts)

a.  RISC  Only loads and stores should reference memory.

b.  ______ Maximize the rate at which memory is referenced.

c.  ______ All instructions should be able to reference memory.

d.  RISC  Instructions should be easy to decode.

e.  ______ Retain backwards compatibility.

f.  RISC  Provide plenty of registers.

g.  ______ All instructions are directly issued by hardware.

h.  ______ Provide plenty of bus bandwidth.

i.  RISC  All instructions are directly executed by hardware.

j.  RISC  Maximize the rate at which instructions are issued.

13. Consider a machine that has a clock time of 8ns and uses a 9-stage pipeline. (8 pts)

a. What is the processor bandwidth in MIPS of this machine? 125 MIPS

b. What is the latency for a single instruction? 72 ns

Compare the pipelined machine above to a machine that does not use pipelining and has a clock time of 20ns.

c. What is the processor bandwidth in MIPS of this non-pipelined machine? 50 MIPS

d. What is the latency for a single instruction on this non-pipelined machine? 20 ns
14. List and define two types of locality. (6 pts)

- **Spatial locality** – words in close physical proximity to the word being read will probably be read also

- **Temporal locality** – a recently read word will probably be read again soon

15. The Hamming algorithm was used to generate the following 12-bit codeword.

   0x6D4

However, a two-bit burst error caused bits eleven and twelve to be received as high. Answer the questions below. (12 pts)

   a. What was the original data byte transmitted in hexadecimal? _____ 0xE4 _____

   b. What bit will the Hamming algorithm attempt to correct? _____ Bit 7 _____

   Parity 1  incorrect
   Parity 2  incorrect  ➔ Error in Bit 7
   Parity 4  incorrect
   Parity 8  correct

   c. What data byte in hexadecimal will be extracted from the corrected codeword due to the undetectable burst error?

     _____ 0xF7 _____