Problem I.  Problem 2.3, Tanenbaum textbook, page 113 (5 points)

From the Tanenbaum Problem Solutions:

You cannot say anything for sure. If computer 1 has a five stage pipeline, it can issue up to 500 million instructions per second. If computer 2 is not pipelined, it cannot do any better than 200 million instructions per second. Thus without more information, you cannot say which is faster.

Problem II.  Problem 2.19, Tanenbaum textbook, page 115 (10 points)

From the Tanenbaum Problem Solutions:

With 4096 bits/sector and 64 sectors/track, each track holds 262,144 bits. At 7200 RPM, each rotation takes 1/120 of a second. In one second it can read 31,457,280 bits for a rate of 3.9 MB/s.

Problem III.  Problem 4.26, Tanenbaum textbook, page 301 (10 points)

From the Tanenbaum Problem Solutions:

The mean access time is $0.8 \times 5 + 0.15 \times 20 + 0.05 \times 80$. This gives 11 ns.
**Problem IV.** Use Hamming’s Algorithm to compute the codewords for the following data values: (20 points)

(a) 0x3D

The codeword is 0x57D

(b) 0x2BAD

The codeword is 0x0AB76D

**Problem V.** Determine if there is an error in the following 12-bit codeword. Write the bit number if an error occurred or write “none” if there is no error. This codeword was generated using Hamming's Algorithm and contains 8 data bits. (10 points)

0x8E3

There is an error in Bit 2. The correct codeword is 0xCE3

**Problem VI.** Using the following list of addresses, give the final state of the direct-mapped cache. Assume the architecture has a 16-bit datapath. Also, a cache line holds 16 words. (20 points)

Address read 1: 0xA5ED
Address read 2: 0x77B7
Address read 3: 0x92FB
Address read 4: 0x2B51

<table>
<thead>
<tr>
<th>Entry</th>
<th>Valid</th>
<th>Tag</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Y</td>
<td>0x2B</td>
</tr>
<tr>
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</tr>
<tr>
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<td>N</td>
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