Problem 1. Problem 2.8, Brown/Vranesic textbook, page 68

2.8. Timing diagram of the waveforms that can be observed on all wires of the circuit:
Problem II.  Problem 2.9, Brown/Vranesic textbook, page 68

2.9. Timing diagram of the waveforms that can be observed on all wires of the circuit:

Problem III.  Problem 2.18, Brown/Vranesic textbook, page 68

2.18. In Figure P2.1a it is possible to represent only 14 minterms. It is impossible to represent the minterms \( \overline{x_1}\overline{x_2}x_3\overline{x_4} \) and \( x_1x_2\overline{x_3}\overline{x_4} \).

In Figure P2.1b, it is impossible to represent the minterms \( x_1x_2\overline{x_3}\overline{x_4} \) and \( x_1x_2x_3\overline{x_4} \).

Problem IV.  Problem 2.28, Brown/Vranesic textbook, page 70

2.28. The lowest-cost circuit is defined by

\[
f(x_1, x_2, x_3) = x_1x_2 + x_1x_3 + x_2x_3\]
Problem V.  Problem 2.30, Brown/Vranesic textbook, page 70

2.30. The circuit can be implemented as

\[ f = x_1 x_2 x_3 \overline{x}_4 + x_1 x_2 \overline{x}_3 x_4 + x_1 \overline{x}_2 x_3 x_4 + \overline{x}_1 x_2 x_3 x_4 + x_1 x_2 x_3 x_4 \]
\[ = x_1 x_2 x_3 (\overline{x}_4 + x_4) + x_1 x_2 (\overline{x}_3 + x_3) x_4 + x_1 (\overline{x}_2 + x_2) x_3 x_4 + (\overline{x}_1 + x_1) x_2 x_3 x_4 \]
\[ = x_1 x_2 x_3 + x_1 x_2 x_4 + x_1 x_3 x_4 + x_2 x_3 x_4 \]

Problem VI.  Problem 2.33, Brown/Vranesic textbook, page 70

2.33. The truth table that corresponds to the timing diagram in Figure P2.4 is

<table>
<thead>
<tr>
<th>( x_1 )</th>
<th>( x_2 )</th>
<th>( x_3 )</th>
<th>( f )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>1</td>
</tr>
</tbody>
</table>

The simplest SOP expression is derived as follows:

\[ f = \overline{x}_1 x_2 x_3 + \overline{x}_1 x_2 \overline{x}_3 + \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 + x_1 x_2 x_3 \]
\[ = \overline{x}_1 (x_2 + x_2) x_3 + \overline{x}_1 x_2 (\overline{x}_3 + x_3) + (\overline{x}_1 + x_1) x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 \]
\[ = \overline{x}_1 \cdot 1 \cdot x_3 + \overline{x}_1 x_2 \cdot 1 + 1 \cdot x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 \]
\[ = \overline{x}_1 x_3 + \overline{x}_1 x_2 + x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 \]
**Problem VII.** Problem 2.34, Brown/Vranesic textbook, page 70

2.34. The truth table that corresponds to the timing diagram in Figure P2.4 is

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$x_3$</th>
<th>$f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>1</td>
</tr>
</tbody>
</table>

The simplest POS expression is $f = (x_1 + x_2 + x_3)(\overline{x_1} + x_2 + \overline{x_3})(\overline{x_1} + \overline{x_2} + x_3)$.

**Problem VIII.** Problem 2.38, Brown/Vranesic textbook, page 71

2.38. Using the circuit in Figure 2.25(b) as a starting point, the function in Figure 2.24 can be implemented using NOR gates as follows:

![Circuit Diagram]

**Problem IX.** Problem 2.45, Brown/Vranesic textbook, page 71

(Should include Quartus II schematic and waveform diagram)
Problem X. Problem 2.46, Brown/Vranesic textbook, page 71

2.46. The function can be specified by using the minterms as follows:

    ENTITY problem46 IS
        PORT ( x1, x2, x3 : IN BIT;
               f : OUT BIT ) ;
    END problem46 ;

    ARCHITECTURE LogicFunc OF problem46 IS
    BEGIN
        f <= (NOT x1 AND NOT x2 AND NOT x3) OR (NOT x1 AND NOT x2 AND x3) OR
             (NOT x1 AND x2 AND x3) OR (x1 AND NOT x2 AND NOT x3) OR
             (x1 AND NOT x2 AND x3) OR (x1 AND x2 AND NOT x3) ;
    END LogicFunc ;

The simplest SOP expression for this function is

\[ f = \overline{x}_2 + x_1\overline{x}_3 + \overline{x}_1x_3 \]

Using this expression, we can replace the statement that specifies \( f \) in the above VHDL code with the statement

\[ f <= \text{NOT } x_2 \text{ OR } (x_1 \text{ AND NOT } x_3) \text{ OR } (\text{NOT } x_1 \text{ AND } x_3) ; \]

Another way of specifying the function is by using the maxterms, \( M_2 \) and \( M_7 \), in which case the VHDL statement would be

\[ f <= (x_1 \text{ OR NOT } x_2 \text{ OR } x_3) \text{ AND } (\text{NOT } x_1 \text{ OR NOT } x_2 \text{ OR NOT } x_3) ; \]