Problem 1. Problem 3.44, Brown/Vranesic textbook, page 159
Problem II. Problem 3.46, Brown/Vranesic textbook, page 159

3.46. The canonical SOP for \( f \) is

\[
f = x_1 x_2 x_4 + x_2 x_3 x_4 + \overline{x_1} \overline{x_2} x_3
\]

This expression can be manipulated into

\[
f = x_2 \cdot (x_1 x_4 + x_3 x_4 \overline{x_1}) + \overline{x_2} \cdot (\overline{x_1} \overline{x_3})
\]

Using functional decomposition we have

\[
f = x_2 f_1 + \overline{x_2} f_2
\]

where

\[
f_1 = x_1 x_4 + x_3 x_4
f_2 = \overline{x_1} \overline{x_3}
\]

The circuit is
Problem III. Problem 3.51, Brown/Vranesic textbook, page 160

3.51. 

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob3_51 IS
  PORT ( x1, x2, x3, x4 : IN STD_LOGIC;
        f : OUT STD_LOGIC ) ;
END prob3_51 ;

ARCHITECTURE LogicFunc OF prob3_51 IS
BEGIN
  f <= (x2 AND NOT x3 AND NOT x4) OR
       (NOT x1 AND x2 AND x4) OR
       (NOT x1 AND x2 AND x3) OR (x1 AND x2 AND x3) ;
END LogicFunc ;

Problem IV. Problem 3.52, Brown/Vranesic textbook, page 161

3.52. 

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob3_52 IS
  PORT ( x1, x2, x3, x4 : IN STD_LOGIC;
        f : OUT STD_LOGIC ) ;
END prob3_52 ;

ARCHITECTURE LogicFunc OF prob3_52 IS
BEGIN
  f <= (x1 OR x2 OR NOT x4) AND
       (NOT x2 OR x3 OR NOT x4) AND
       (NOT x1 OR x3 OR NOT x4) AND
       (NOT x1 OR NOT x3 OR NOT x4) ;
END LogicFunc ;

Problem V. Problem 3.54, Brown/Vranesic textbook, page 161

3.54. The circuit in Figure P3.10 is a two-input XOR gate. Since NMOS transistors are used only to pass logic 0 and PMOS transistors are used only to pass logic 1, the circuit does not suffer from any major drawbacks.